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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/707,840 | 01/16/2004 | Huilong Zhu | FIS920030237 | 1839 |

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MCGUIRE WOODS LLP
1750 TYSONS BLVD.
SUITE 1800
MCLEAN, VA 22102-4215

| EXAMINER | |
|---|---|
| NGUYEN, DAO H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/707,840 | ZHU ET AL. | |
| | Examiner | Art Unit | |
| | Dao H. Nguyen | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11,13-15 and 29-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,29-31 and 35-46* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) *13-15 and 32-34* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0506*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is in response to the communications dated 05/09/2006.

Claims 1-11, 13-15, and 29-46 are active in this application.

Claim(s) 12 and 16-28 have been cancelled.

New claim(s) 35-46 have been added.

### Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 05/09/2006. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

### Withdrawal of Allowability

3. The indicated allowability of claims 1-11, 13-15, and 29-34 is withdrawn in view of the newly discovered reference(s) to Yu (US Patent No. 6,248,637). Rejections based on the newly cited reference(s) follow.

### Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**5. Claim(s) 1-7 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,248,637 to Yu.**

Regarding claim 1, Yu discloses a method of fabricating a semiconductor structure, as illustrated in figs. 1-8, comprising the steps of:

forming a raised source region 22 on a substrate 14;

forming a raised drain region 24 on the substrate 14; and

forming a first silicon layer 53 (see col. 5, lines 53-59) over the raised source region 22 and a second silicon layer 53 over the raised drain region 24,

wherein the first silicon layer 53 formed over the raised source region 22 and the second silicon layer 53 over the raised drain region 24 include cap portions (top portion of layer 53) and sidewall portions, the method further comprising a step of forming sacrificial spacers 92 along the silicon sidewall portions (facing the gate 36).

Regarding claim 2, Yu discloses the method wherein the substrate 14 includes a SiGe layer atop a buried oxide layer. See col. 3, line 66 to col. 4, line 3.

Regarding claim 3, Yu discloses the method further comprising a step of forming a gate stack 36 on the substrate 14. See fig. 2.

Regarding claim 4, Yu discloses the method further comprising a step of forming a trench isolation 52 surrounding the gate stack 36, source region 22 and drain region 24. See figs. 1-8.

Regarding claim 5, Yu discloses the method further comprising a step of forming a first silicide contact 56 on the first silicon layer. See col. 6, lines 10-16.

Regarding claim 6, Yu discloses the method further comprising a step of forming a second silicide contact 56 on the second silicon layer. See col. 6, lines 10-16.

Regarding claim 7, Yu discloses the method wherein the first silicon layer is epitaxially formed silicon and the second silicon layer is epitaxially grown silicon. See col. 5, lines 53-59.

**6. Claim(s) 29-31 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,955,770 to Chan et al.**

Regarding claim 29, Chan discloses a method of fabricating a semiconductor structure, as shown in figs. 3-6, comprising:

forming a raised source region 77 on a substrate 50;

forming a raised drain region 77 on the substrate 50;

forming a strained silicon layer 80 on the raised source/drain regions 77; and

forming a silicon cap 82 on the strained silicon layer 80.

Regarding claim 30, Chan discloses the method further comprising forming silicon sidewalls on the raised source region and the raised drain region (figs. 5-6 show the silicon layer 80 covering the sidewalls of the raised source/drain regions 77.

Regarding claim 31, Chan discloses the method further comprising forming sacrificial spacers 74 along the silicon sidewalls. See figs. 3-6.

## Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**8. Claim(s) 8-11 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,248,637 to Yu, in view of Zhu et al., US Patent No. 6,939,751.**

Regarding claims 8 and 10, Yu discloses the method comprising all claimed limitations, except for the raised source/drain regions being comprised of a strained silicon layer atop a SiGe layer.

Zhu discloses a method of fabricating a semiconductor structure having raised source/drain regions 16&18 comprising strained silicon layer 18 atop a SiGe layer 16 formed on an SOI substrate. See col. 5, lines 26-65.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Yu so that the source/drain regions would comprising strained silicon layer atop a SiGe layer formed on an SOI substrate, as that of Zhu, in order to increase the device performance due to the great characteristics of SiGe and of SOI substrate. See also col. 6, lines 51-55 of Zhu.

Regarding claims 9 and 11, Yu/Zhu discloses a method wherein the strained silicon layer 18 is comprised of epitaxially grown silicon. See col. 5, lines 27-65 of Zhu.

**9. Claim(s) 35-46 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,955,770 to Chan et al., in view of Zhu et al., US Patent No. 6,939,751.**

Regarding claim 35, Chan discloses a method of fabricating a semiconductor structure, comprising:

providing a substrate 50 having a patterned gate stack region 64 comprising a gate dielectric 62 (fig. 6) formed on a surface thereof,

providing isolation structures 52 on sides of the patterned gate stack region 64;

forming a gate stack 64 on the gate dielectric 62;

forming spacers 74 along gate sidewalls of the gate stack 64;

after spacer formation, forming raised source and drain regions 77;

forming a silicon layer 80 on the raised source and drain regions 77; and

capping the raised drain region with cap 82.

Chan fails to teach that the substrate being an SOI substrate; that the raised source/drain regions comprising an SiGe layer; and that the silicon layer has a smaller lattice constant than Ge such that the silicon layer is strained in tension.

Zhu discloses a method of fabricating a semiconductor structure having an SOI substrate on which raised source/drain regions 16 comprising SiGe and a silicon layer 18 on the SiGe layer 16 (figs. 1); wherein the silicon layer has a smaller lattice constant

than Ge such that the silicon layer is strained in tension. See col. 5, line 26 to col. 6, line 55.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Chan to have raised source/drain regions comprising SiGe layer formed on an SOI substrate, and a silicon layer formed on the SiGe layer, wherein the silicon layer has a smaller lattice constant than Ge such that the silicon layer is strained in tension, as that of Zhu, in order to increase the device performance due to the great characteristics of SiGe and of SOI substrate. See also col. 6, lines 51-55 of Zhu.

Regarding claim 36, Chan/Zhu disclose the method wherein the SOI substrate includes a buried oxide layer (BOX) sandwiched between a top Si-containing layer and a bottom Si-containing layer. See col. 3, lines 17-21 of Zhu.

Regarding claim 37, Chan /Zhu discloses the method wherein the top Si-containing layer and the bottom Si-containing layer comprise Si, SiGe, SiC, SiGeC, Si/si or Si/SiGe. See col. 3, lines 17-21 of Zhu.

Regarding claim 38, Chan/Zhu do/does not necessarily nor expressly discuss about how to form the SOI substrate. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the SOI substrate

of Chan/Zhu can be formed by any suitable conventional methods, including such well known methods as bonding and cutting processes or separation by implantation of oxygen (SIMOX) process. See the specification, paragraph [0018] of the instance application.

Regarding claim 39, Chan/Zhu disclose the method further comprising forming a dielectric-capping layer 66 on the gate stack 64 comprising an oxide, nitride or oxynitride. See col. 3, line 65 to col. 4, line 12 of Chan.

Regarding claim 40, Chan/Zhu discloses the method wherein the SiGe layer of the source and drain regions are selectively epitaxially grown. See col. 4, lines 21-61 of Chan.

Regarding claim 41, Chan/Zhu disclose the method wherein the SiGe layer of the source and drain regions are comprised, in whole or in part, of a top silicon-containing layer of the SOI substrate. See figs. 1-3 of Zhu.

Regarding claim 42, Chan/Zhu disclose the method wherein a thickness for the strained Si layer on top of the SiGe layer is below a critical thickness. See col. 4, line 21 to col. 5, line 44 of Chan.

Regarding claim 43, Chan/Zhu disclose the method wherein the critical thickness is a maximum thickness that the strained silicon layer can grow on the SiGe layer without forming defects in a crystal structure. See col. 4, line 21 to col. 5, line 44 of Chan.

Regarding claim 44, Chan/Zhu disclose the method wherein the capping 82 is formed from a silicon capping layer. See col. 5, lines 9-60 of Chan.

Regarding claim 45, Chan/Zhu disclose the method wherein the silicon capping layer is selectively epitaxially grown on the SiGe sidewalls of the raised drain region forming protective sidewalls. See figs. 1-3 of Chan.

Regarding claim 46, Chan/Zhu disclose the method further comprising forming oxide portions 74 alongside the raised drain comprised of the SiGe layer and the strained Si layer. See fig. 6 of Chan.

**Allowable Subject Matter**

10. Claim(s) 13-15, and 32-34 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed

method of fabricating a semiconductor structure further comprising steps of forming a third silicon layer over the cap of the first silicon layer over the raised source region, and forming a fourth silicon layer over the cap of the second silicon layer over the raised drain region (claim 13); nor forming a silicon layer on the silicon cap (claim 32).

## Conclusion

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Dao H. Nguyen
Art Unit 2818
July 9, 2006

DOUGLAS W. OWENS
PRIMARY EXAMINER